# CLAIMS

1. In a memory device having first and second memory arrays sharing sense amplifiers of a sense amplifier region, each memory array having memory cells arranged in rows and columns of memory cells, a column of memory cells comprising:

first and second digit lines coupled to a sense amplifier, each digit line having first and second digit line portions, the first digit line portions of the first and second digit lines associated with the first memory array, the second digit line portions of the first digit line associated with the first memory array, and the second digit line portion of the second digit line associated with the second memory array; and

a plurality of memory cells coupled to the first and second digit lines.

2. The column of memory cells of claim 1 wherein the first digit line portions of the first and second digit lines comprise buried digit lines and the second digit line portions of the first and second digit lines comprise digit lines formed from a metal material.

3. The column of memory cells of claim 1 wherein the plurality of memory cells coupled to the first digit line portions comprises a plurality of memory cells having a $6F^2$ semiconductor structure.

4. The column of memory cells of claim 1 wherein the first digit line portions of the first and second digit lines comprise digit lines formed from a first conductive material and the second digit line portions of the first and second digit lines comprise digit lines formed from a second conductive material.

5. The column of memory cells of claim 1 wherein the first digit line is coupled to the sense amplifier through an isolation switch formed adjacent to the first memory

array and the second digit line is coupled to the sense amplifier through an isolation switch formed adjacent to the second memory array.

6. The column of memory cells of claim 1 wherein the plurality of memory cells comprises a plurality of memory cells coupled to the first portions of the first and second digit lines.

7. The column of memory cells of claim 1 wherein the first portion of the second digit line is coupled to the sense amplifier through the second portion of the second digit line.

8. A digit line architecture for an array of memory cells having at least two memory sub-arrays in which the memory cells are arranged in rows and columns, and the two memory sub-arrays share sense amplifiers of a sense amplifier region separating the two memory sub-arrays, the digit line architecture comprising:

first and second digit lines having first and second digit line segments, the memory cells of a column coupled to the first digit line segments, the second digit line segment of the first digit line located in the memory sub-array with which the column is associated and the second digit line segment of the second digit line extending into the other memory sub-array with which the column is not associated.

9. A semiconductor memory array, comprising:

a sense amplifier region having a plurality of sense amplifiers located therein; and

first and second memory cell regions in which memory cells are arranged in rows and columns of memory cells, the first and second memory cell regions disposed on opposite sides of the sense amplifier region and having columns of memory coupled to a respective sense amplifier, each column of memory having first and second digit lines having first and second digit line segments, the columns of memory of the first memory cell region having the first digit

line segments of the first and second digit lines disposed in the first memory cell region, the second digit line segment of the first digit line disposed in the first memory cell region, and the second digit line segment of the second digit line disposed in the second memory cell region.

10. The semiconductor memory array of claim 9 wherein the columns of memory of the second memory cell region comprise first and second digit lines having first and second digit line segments, the first digit line segments of the first and second digit lines of the columns of the second memory cell region disposed in the second memory cell region, the second digit line segment of the first digit line of the columns of the second memory cell region disposed in the second memory cell region, and the second digit line segment of the second digit line of the columns of the second memory cell region disposed in the first memory cell region.

11. The semiconductor memory array of claim 9 wherein the first digit line segments of the first and second digit lines of a column of memory comprise buried digit lines and the second digit lines segments of the first and second digit lines of a column of memory comprise digit lines formed from a metal material.

12. The semiconductor memory array of claim 9 wherein the memory cells of the first and second memory cell regions comprise memory cells having a $6F^2$ semiconductor structure.

13. The semiconductor memory array of claim 9 wherein the first digit line segments of the first and second digit lines of a column of memory comprise digit lines formed from a first conductive material and the second digit line portions of the first and second digit lines of a column comprise digit lines formed from a second conductive material.

14. The semiconductor memory array of claim 9 wherein the first digit line of a column of memory is coupled to a respective sense amplifier through an isolation switch

formed adjacent to the first memory cell region and the second digit line of a column is coupled to the sense amplifier through an isolation switch formed adjacent to the second memory cell region.

15. The semiconductor memory array of claim 9 wherein the memory cells of the first and second memory cell regions comprise memory cells coupled to the first portions of the first and second digit lines of the columns of memory.

16. The semiconductor memory array of claim 9 wherein the first portion of the second digit line of a column of memory is coupled to a respective sense amplifier through the second portion of the second digit line.

17. The semiconductor memory array of claim 9 wherein the first segments of the first and second digit lines of a column of memory extend across approximately one-half of the memory cell region in which the column is located.

18. A memory array, comprising:

first and second memory sub-arrays of memory cells, the memory cells of each sub-array arranged in rows and columns of memory cells, each column of memory having first and second digit lines coupled to a sense amplifier, each digit line having first and second digit line portions, the columns of memory of the first memory sub-array having the first digit line portions of the first and second digit lines associated with the first memory sub-array, the second digit line portions of the first digit line associated with the first memory array, and the second digit line portion of the second digit line associated with the second memory sub-array.

19. The memory array of claim 18 wherein the columns of memory of the second memory sub-array comprise first and second digit lines having first and second digit line portions, the first digit line segments of the first and second digit lines of the columns of the

second memory sub-array disposed in the second memory cell region, the second digit line segment of the first digit line of the columns of the second memory sub-array disposed in the second memory cell region, and the second digit line segment of the second digit line of the columns of the second memory sub-array disposed in the first memory cell region.

20. The memory array of claim 18 wherein the first digit line segments of the first and second digit lines of a column of memory comprise buried digit lines and the second digit lines segments of the first and second digit lines of a column of memory comprise digit lines formed from a metal material.

21. The memory array of claim 18 wherein the memory cells of the first and second memory sub-arrays comprise memory cells having a $6F^2$ semiconductor structure.

22. The memory array of claim 18 wherein the first digit line segments of the first and second digit lines of a column of memory comprise digit lines formed from a first conductive material and the second digit line portions of the first and second digit lines of a column comprise digit lines formed from a second conductive material.

23. The memory array of claim 18 wherein the first digit line of a column of memory is coupled to a respective sense amplifier through an isolation switch formed adjacent to the first memory sub-array and the second digit line of a column is coupled to the sense amplifier through an isolation switch formed adjacent to the second memory sub-array.

24. The memory array of claim 18 wherein the memory cells of the first and second memory sub-arrays comprise memory cells coupled to the first portions of the first and second digit lines of the columns of memory.

25. The memory array of claim 18 wherein the first portion of the second digit line of a column of memory is coupled to a respective sense amplifier through the second portion of the second digit line.

26. The memory array of claim 18 wherein the first segments of the first and second digit lines of a column of memory extend across approximately one-half of the memory sub-array in which the column is located.

27. A memory device, comprising:

a memory array having first and second memory sub-arrays of memory cells, the memory cells of each sub-array arranged in rows and columns of memory cells, each column of memory having first and second digit lines coupled to a sense amplifier, each digit line having first and second digit line portions, the columns of memory of the first memory sub-array having the first digit line portions of the first and second digit lines associated with the first memory sub-array, the second digit line portions of the first digit line associated with the first memory array, and the second digit line portion of the second digit line associated with the second memory sub-array;

an address decoder receiving a memory address at an external terminal, the address decoder being operable to activate a row and column in the array corresponding to the memory address; and

a data path operable to couple read data from an external terminal to the memory array and write data from the memory array to the external terminal.

28. The memory device of claim 27 wherein the columns of memory of the second memory sub-array comprise first and second digit lines having first and second digit line portions, the first digit line segments of the first and second digit lines of the columns of the second memory sub-array disposed in the second memory cell region, the second digit line segment of the first digit line of the columns of the second memory sub-array disposed in the

second memory cell region, and the second digit line segment of the second digit line of the columns of the second memory sub-array disposed in the first memory cell region.

29. The memory device of claim 27 wherein the first digit line segments of the first and second digit lines of a column of memory of the memory array comprise buried digit lines and the second digit lines segments of the first and second digit lines of a column of memory comprise digit lines formed from a metal material.

30. The memory device of claim 27 wherein the memory cells of the first and second memory sub-arrays of the memory array comprise memory cells having a $6F^2$ semiconductor structure.

31. The memory device of claim 27 wherein the first digit line segments of the first and second digit lines of a column of memory of the memory array comprise digit lines formed from a first conductive material and the second digit line portions of the first and second digit lines of a column comprise digit lines formed from a second conductive material.

32. The memory device of claim 27 wherein the first digit line of a column of memory of the memory array is coupled to a respective sense amplifier through an isolation switch formed adjacent to the first memory sub-array and the second digit line of a column is coupled to the sense amplifier through an isolation switch formed adjacent to the second memory sub-array.

33. The memory device of claim 27 wherein the memory cells of the first and second memory sub-arrays of the memory array comprise memory cells coupled to the first portions of the first and second digit lines of the columns of memory.

34. The memory device of claim 27 wherein the first portion of the second digit line of a column of memory of the memory array is coupled to a respective sense amplifier through the second portion of the second digit line.

35. The memory device of claim 27 wherein the first segments of the first and second digit lines of a column of memory of the memory array extend across approximately one-half of the memory sub-array in which the column is located.

36. A computer system, comprising:

a processor;

a peripheral device bus; and

a memory device, comprising:

a memory array having first and second memory sub-arrays of memory cells, the memory cells of each sub-array arranged in rows and columns of memory cells, each column of memory having first and second digit lines coupled to a sense amplifier, each digit line having first and second digit line portions, the columns of memory of the first memory sub-array having the first digit line portions of the first and second digit lines associated with the first memory sub-array, the second digit line portions of the first digit line associated with the first memory array, and the second digit line portion of the second digit line associated with the second memory sub-array;

an address decoder receiving a memory address at an external terminal, the address decoder being operable to activate a row and column in the array corresponding to the memory address; and

a data path operable to couple read data from an external terminal to the memory array and write data from the memory array to the external terminal.

37. The computer system of claim 36 wherein the columns of memory of the second memory sub-array comprise first and second digit lines having first and second digit line

portions, the first digit line segments of the first and second digit lines of the columns of the second memory sub-array disposed in the second memory cell region, the second digit line segment of the first digit line of the columns of the second memory sub-array disposed in the second memory cell region, and the second digit line segment of the second digit line of the columns of the second memory sub-array disposed in the first memory cell region.

38. The computer system of claim 36 wherein the first digit line segments of the first and second digit lines of a column of memory of the memory array comprise buried digit lines and the second digit lines segments of the first and second digit lines of a column of memory comprise digit lines formed from a metal material.

39. The computer system of claim 36 wherein the memory cells of the first and second memory sub-arrays of the memory array comprise memory cells having a $6F^2$ semiconductor structure.

40. The computer system of claim 36 wherein the first digit line segments of the first and second digit lines of a column of memory of the memory array comprise digit lines formed from a first conductive material and the second digit line portions of the first and second digit lines of a column comprise digit lines formed from a second conductive material.

41. The computer system of claim 36 wherein the first digit line of a column of memory of the memory array is coupled to a respective sense amplifier through an isolation switch formed adjacent to the first memory sub-array and the second digit line of a column is coupled to the sense amplifier through an isolation switch formed adjacent to the second memory sub-array.

42. The computer system of claim 36 wherein the memory cells of the first and second memory sub-arrays of the memory array comprise memory cells coupled to the first portions of the first and second digit lines of the columns of memory.

43. The computer system of claim 36 wherein the first portion of the second digit line of a column of memory of the memory array is coupled to a respective sense amplifier through the second portion of the second digit line.

44. The computer system of claim 36 wherein the first segments of the first and second digit lines of a column of memory of the memory array extend across approximately one-half of the memory sub-array in which the column is located.

45. A method for forming columns of memory cells having first and second digit lines for an array of memory cells, the method comprising:

forming first digit line segments to which the memory cells are coupled of the first and second digit lines in a first memory array region;

forming a second digit line segment of the first digit line in the first memory array region; and

forming a second digit line segment of the second digit line extending into a second memory array region non-adjoining the first memory array region

46. The method of claim 45 wherein forming the first digit line segments comprises forming buried digit lines.

47. The method of claim 45 wherein forming the second digit line segments comprises forming a digit line segment from a metal material.

48. The method of claim 45 wherein forming the first digit line segments comprises forming a digit line segment from a first conductive material and forming the second digit line segments comprises forming a digit line segment from a second conductive material.

49. The method of claim 45 wherein forming the first digit line segments comprises forming first digit line segments extending across substantially one-half of the memory array in which the first digit line segment is located.

50. A method for sensing a column of memory cells for an array of memory cells having at least first and second memory sub-arrays in which the memory cells are arranged in rows and columns, the method comprising:

activating a row of memory of the first memory sub-array;

coupling a first digit line of the column of memory cells in the first memory sub-array to a respective sense amplifier, the first digit line having a first digit line portion to which memory cells of the column are coupled and further having a second digit line portion, both digit line portions located in the first memory sub-array;

coupling a second digit line of the column of memory cells in the first memory sub-array to the respective sense amplifier, the second digit line having a first digit line portion to which memory cells of the column located in the first memory sub-array and further having a second digit line portion extending into the second memory sub-array; and

detecting and amplifying a voltage difference between the first and second digit lines.

51. The method of claim 50 wherein the first digit line portions comprise forming buried digit lines.

52. The method of claim 50 wherein the second digit line portions comprise forming a digit line segment from a metal material.

53. The method of claim 50 wherein the first digit line portions comprise digit line portions formed from a first conductive material and the second digit line portions of the first and second digit lines comprise digit line portions formed from a second conductive material.

54. The method of claim 50 wherein the first digit line portions comprise forming first digit line segments extending across substantially one-half of the memory array in which the first digit line segment is located.